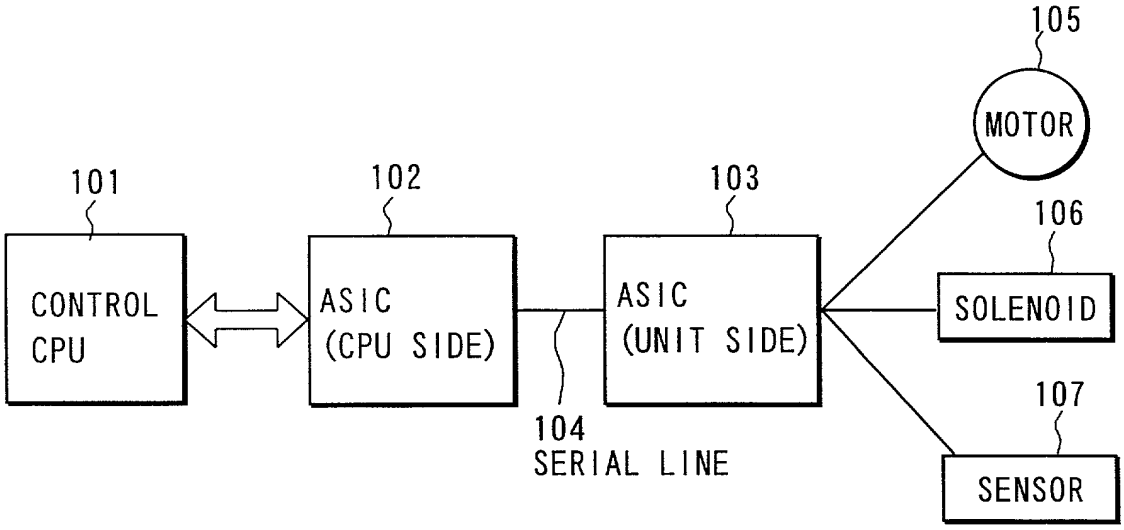
105
MOTOR
101
102
103
106
CONTROL CPU
ASIC (CPU SIDE)
ASIC (UNIT SIDE)
SOLENOID
107
104
SERIAL LINE
SENSOR

FIG. 1

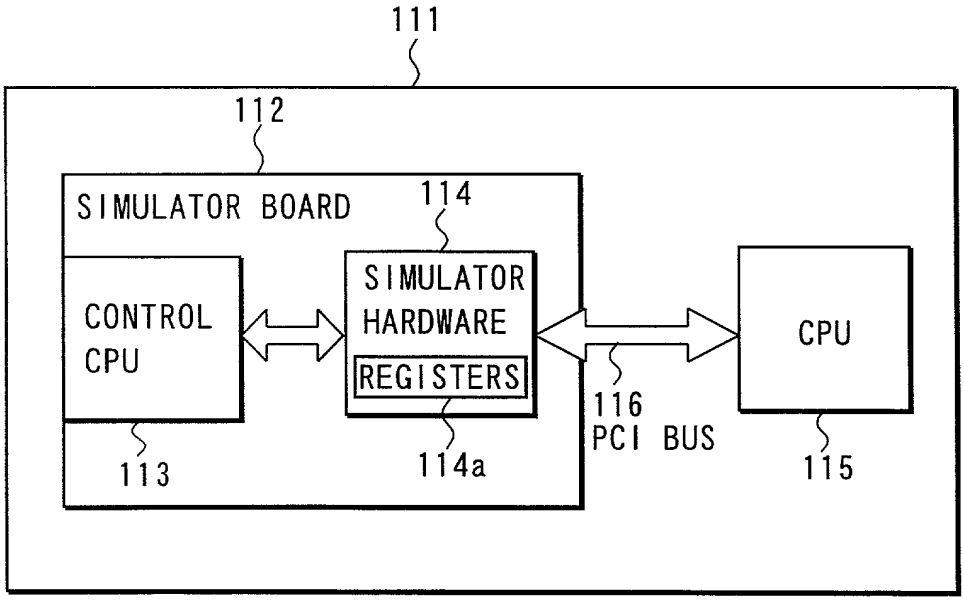
111
112
SIMULATOR BOARD
114
CONTROL CPU
SIMULATOR HARDWARE
REGISTERS
CPU
116
PCI BUS
113
114a
115

FIG. 2

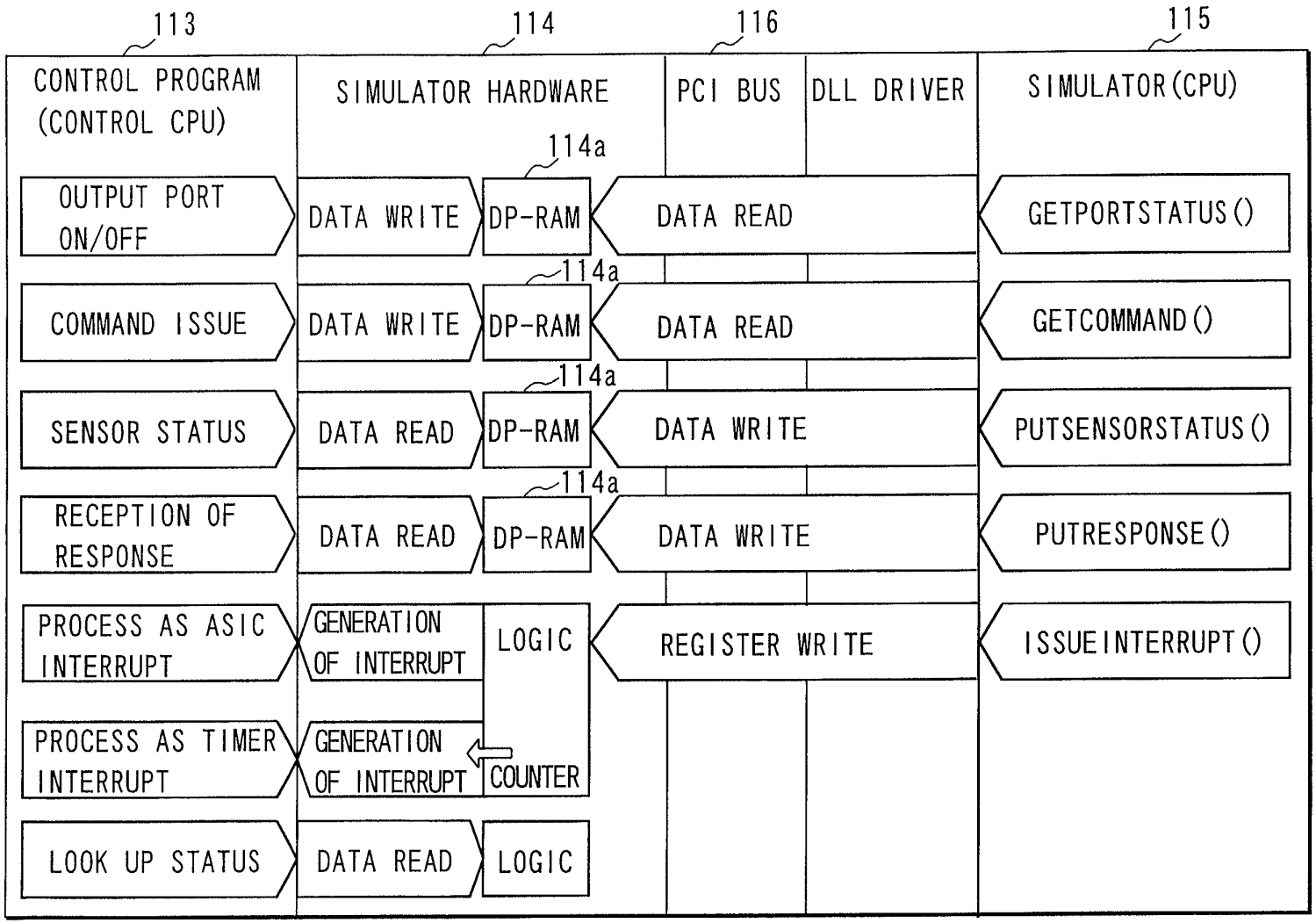
113
114
116
115
CONTROL PROGRAM (CONTROL CPU)
SIMULATOR HARDWARE
PCI BUS
DLL DRIVER
SIMULATOR(CPU)
114a
OUTPUT PORT ON/OFF
DATA WRITE
DP-RAM
DATA READ
GETPORTSTATUS()
COMMAND ISSUE
DATA WRITE
DP-RAM
DATA READ
GETCOMMAND()
SENSOR STATUS
DATA READ
DP-RAM
DATA WRITE
PUTSENSORSTATUS()
RECEPTION OF RESPONSE
DATA READ
DP-RAM
DATA WRITE
PUTRESPONSE()
PROCESS AS ASIC INTERRUPT
GENERATION OF INTERRUPT
LOGIC
REGISTER WRITE
ISSUEINTERRUPT()
PROCESS AS TIMER INTERRUPT
GENERATION OF INTERRUPT
COUNTER
LOOK UP STATUS
DATA READ
LOGIC

FIG. 3A

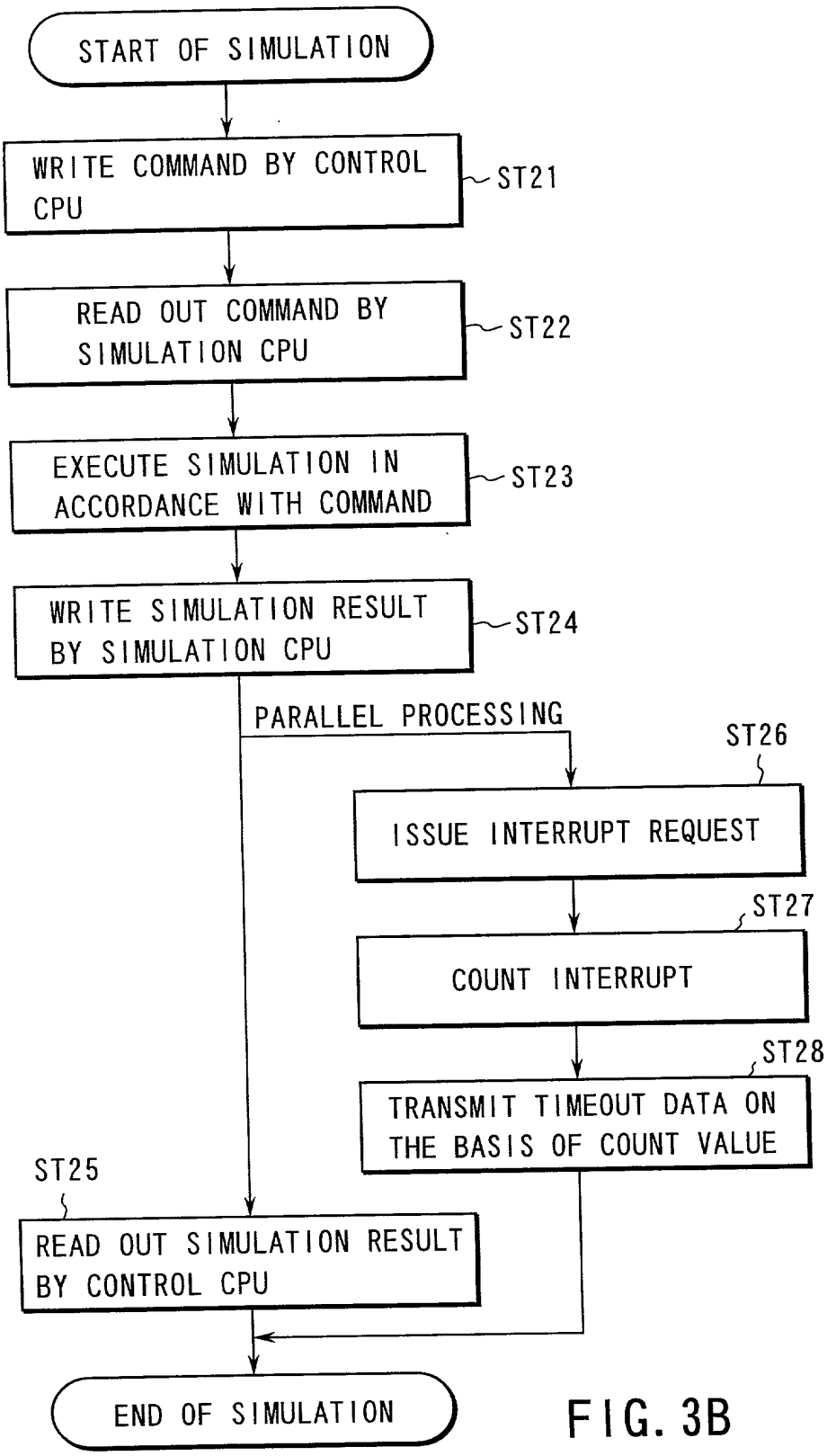
START OF SIMULATION
WRITE COMMAND BY CONTROL CPU
ST21
READ OUT COMMAND BY SIMULATION CPU
ST22
EXECUTE SIMULATION IN ACCORDANCE WITH COMMAND
ST23
WRITE SIMULATION RESULT BY SIMULATION CPU
ST24
PARALLEL PROCESSING
ST26
ISSUE INTERRUPT REQUEST
ST27
COUNT INTERRUPT
ST28
TRANSMIT TIMEOUT DATA ON THE BASIS OF COUNT VALUE
ST25
READ OUT SIMULATION RESULT BY CONTROL CPU
END OF SIMULATION

FIG. 3B

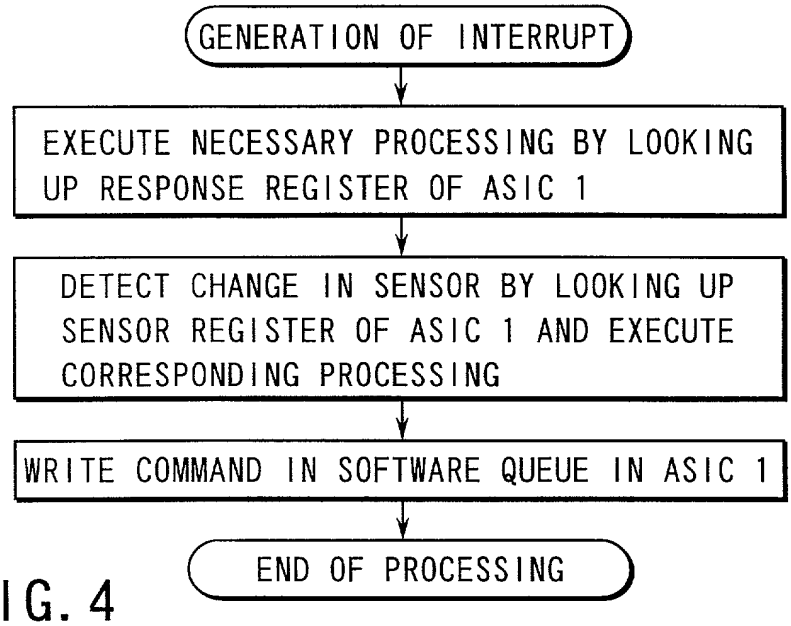
GENERATION OF INTERRUPT
EXECUTE NECESSARY PROCESSING BY LOOKING UP RESPONSE REGISTER OF ASIC 1
DETECT CHANGE IN SENSOR BY LOOKING UP SENSOR REGISTER OF ASIC 1 AND EXECUTE CORRESPONDING PROCESSING
WRITE COMMAND IN SOFTWARE QUEUE IN ASIC 1
END OF PROCESSING

FIG. 4

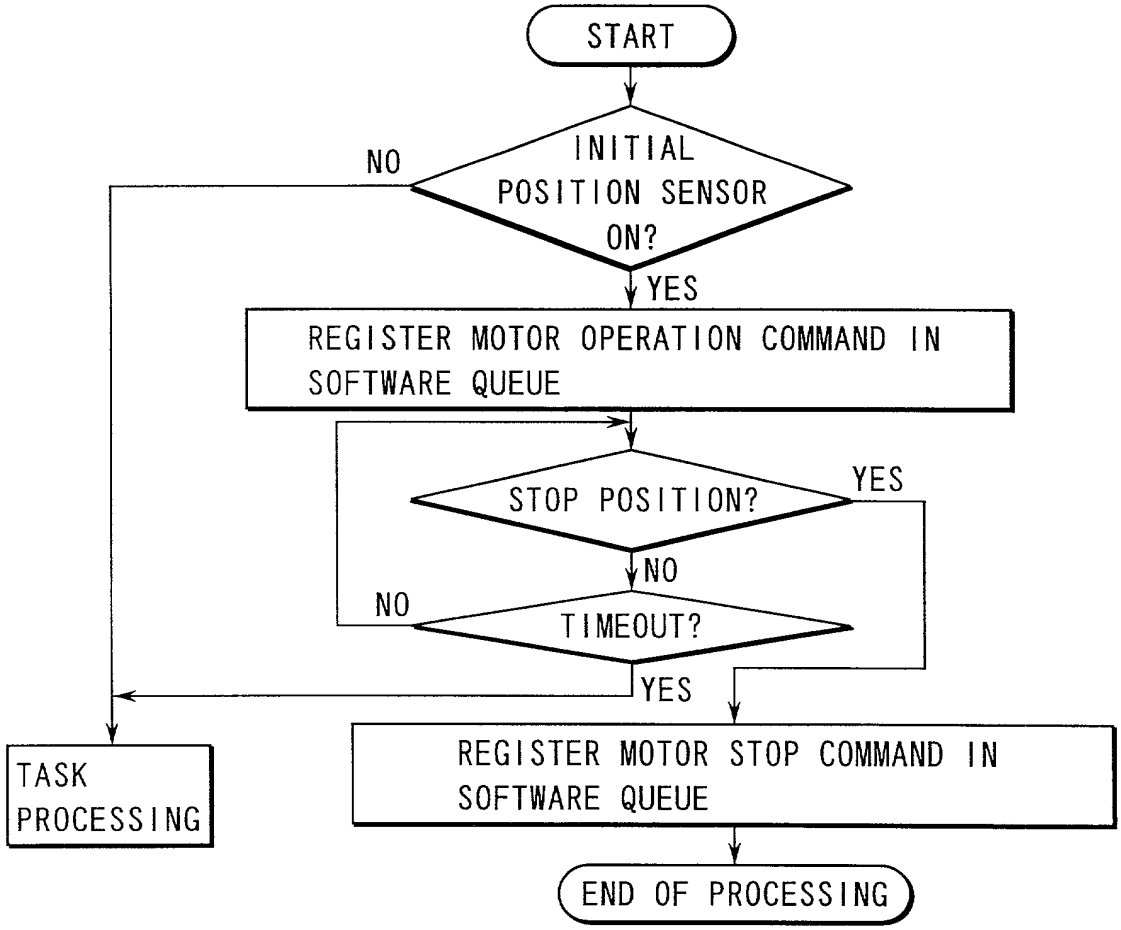
START
INITIAL POSITION SENSOR ON?
NO
YES
REGISTER MOTOR OPERATION COMMAND IN SOFTWARE QUEUE
STOP POSITION?
YES
NO
TIMEOUT?
NO
YES
TASK PROCESSING
REGISTER MOTOR STOP COMMAND IN SOFTWARE QUEUE
END OF PROCESSING

FIG. 5

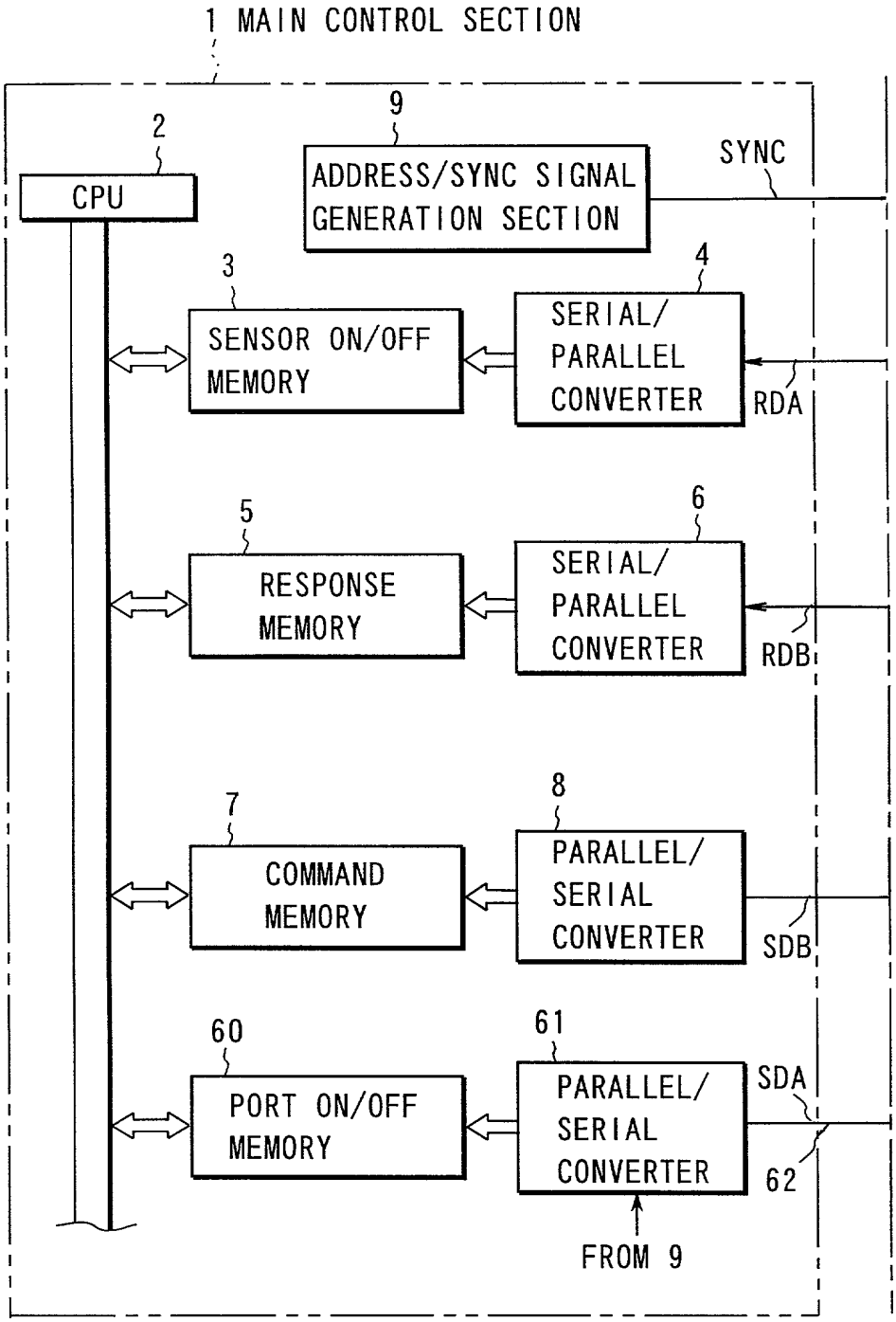
1 MAIN CONTROL SECTION
2
CPU
9
ADDRESS/SYNC SIGNAL GENERATION SECTION
SYNC
3
SENSOR ON/OFF MEMORY
4
SERIAL/ PARALLEL CONVERTER
RDA
5
RESPONSE MEMORY
6
SERIAL/ PARALLEL CONVERTER
RDB
7
COMMAND MEMORY
8
PARALLEL/ SERIAL CONVERTER
SDB
60
PORT ON/OFF MEMORY
61
PARALLEL/ SERIAL CONVERTER
SDA
62
FROM 9

FIG. 6A

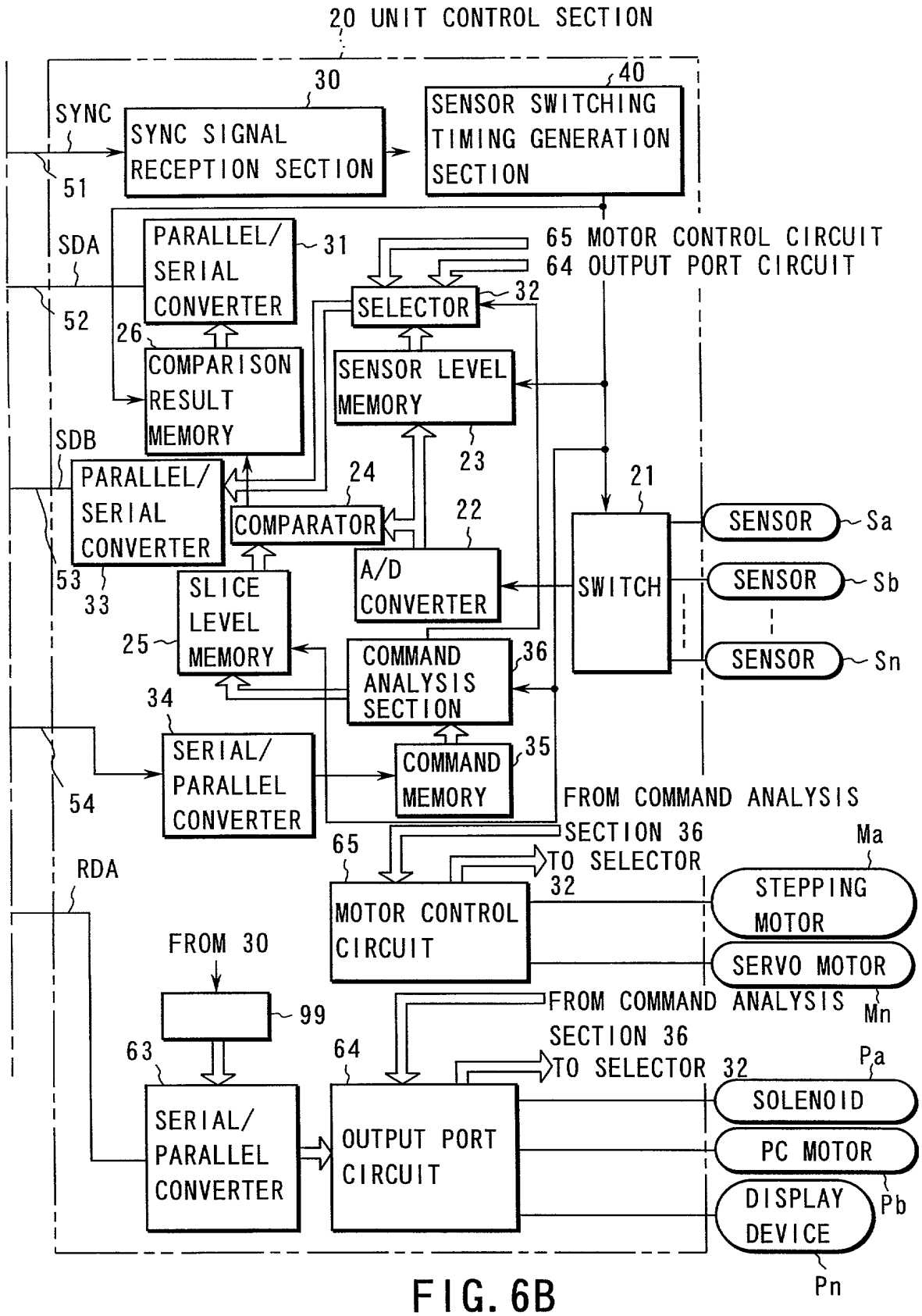
20 UNIT CONTROL SECTION
30
SYNC
SYNC SIGNAL RECEPTION SECTION
40
SENSOR SWITCHING TIMING GENERATION SECTION
51
SDA
PARALLEL/ SERIAL CONVERTER
31
65 MOTOR CONTROL CIRCUIT
64 OUTPUT PORT CIRCUIT
SELECTOR
32
52
26
COMPARISON RESULT MEMORY
SENSOR LEVEL MEMORY
23
SDB
PARALLEL/ SERIAL CONVERTER
24
COMPARATOR
22
21
SENSOR
Sa
SENSOR
Sb
SENSOR
Sn
A/D CONVERTER
SWITCH
53
33
SLICE LEVEL MEMORY
25
COMMAND ANALYSIS SECTION
36
34
SERIAL/ PARALLEL CONVERTER
COMMAND MEMORY
35
54
FROM COMMAND ANALYSIS SECTION 36 TO SELECTOR 32
65
Ma
RDA
MOTOR CONTROL CIRCUIT
32
STEPPING MOTOR
SERVO MOTOR
FROM 30
99
FROM COMMAND ANALYSIS SECTION 36 TO SELECTOR 32
Mn
63
64
Pa
SERIAL/ PARALLEL CONVERTER
OUTPUT PORT CIRCUIT
SOLENOID
PC MOTOR
DISPLAY DEVICE
Pb
Pn

FIG. 6B

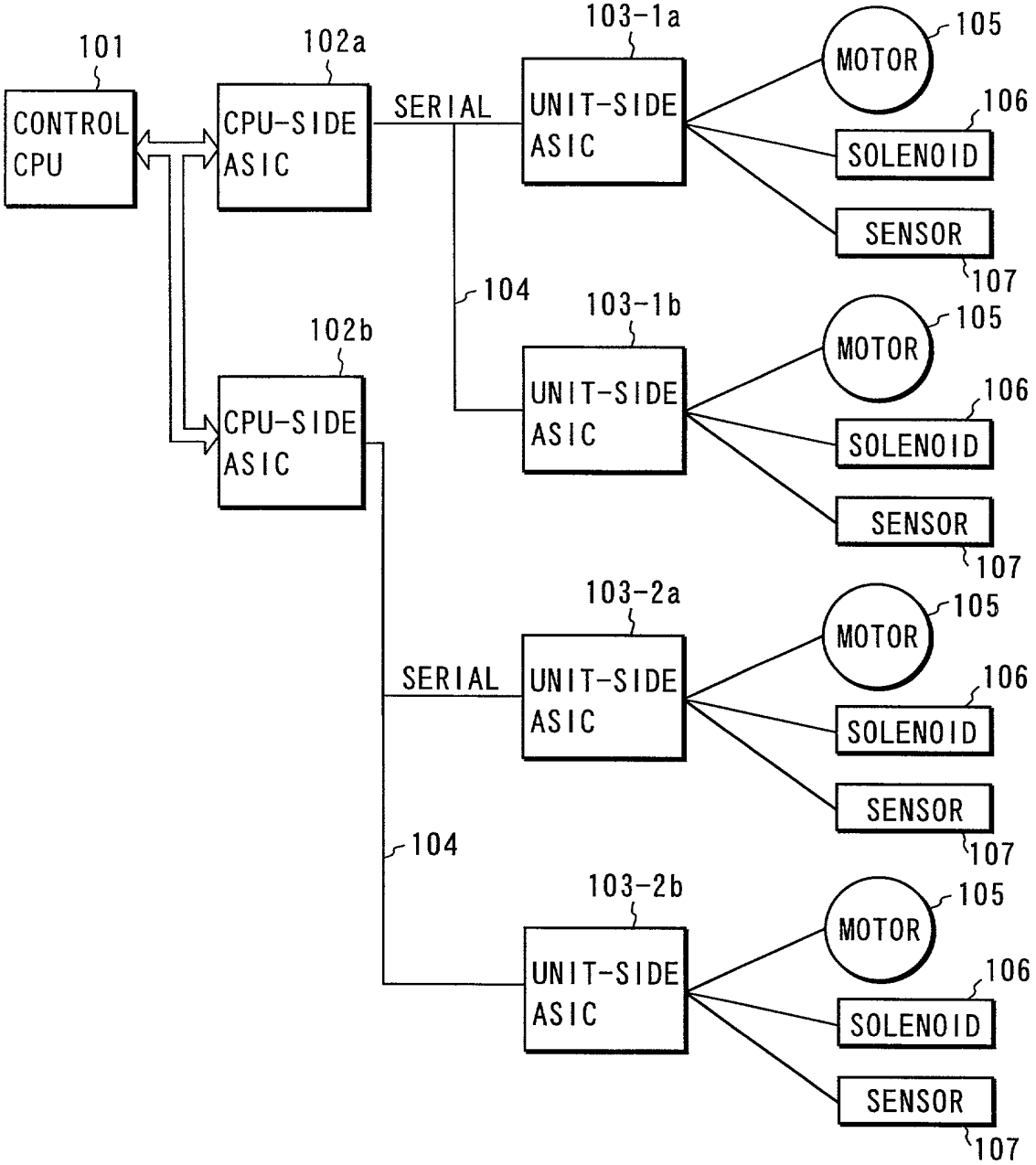
101
CONTROL CPU
102a
CPU-SIDE ASIC
SERIAL
103-1a
UNIT-SIDE ASIC
MOTOR
105
SOLENOID
106
SENSOR
107
104
102b
CPU-SIDE ASIC
103-1b
UNIT-SIDE ASIC
MOTOR
105
SOLENOID
106
SENSOR
107
SERIAL
103-2a
UNIT-SIDE ASIC
MOTOR
105
SOLENOID
106
SENSOR
107
104
103-2b
UNIT-SIDE ASIC
MOTOR
105
SOLENOID
106
SENSOR
107

FIG. 7

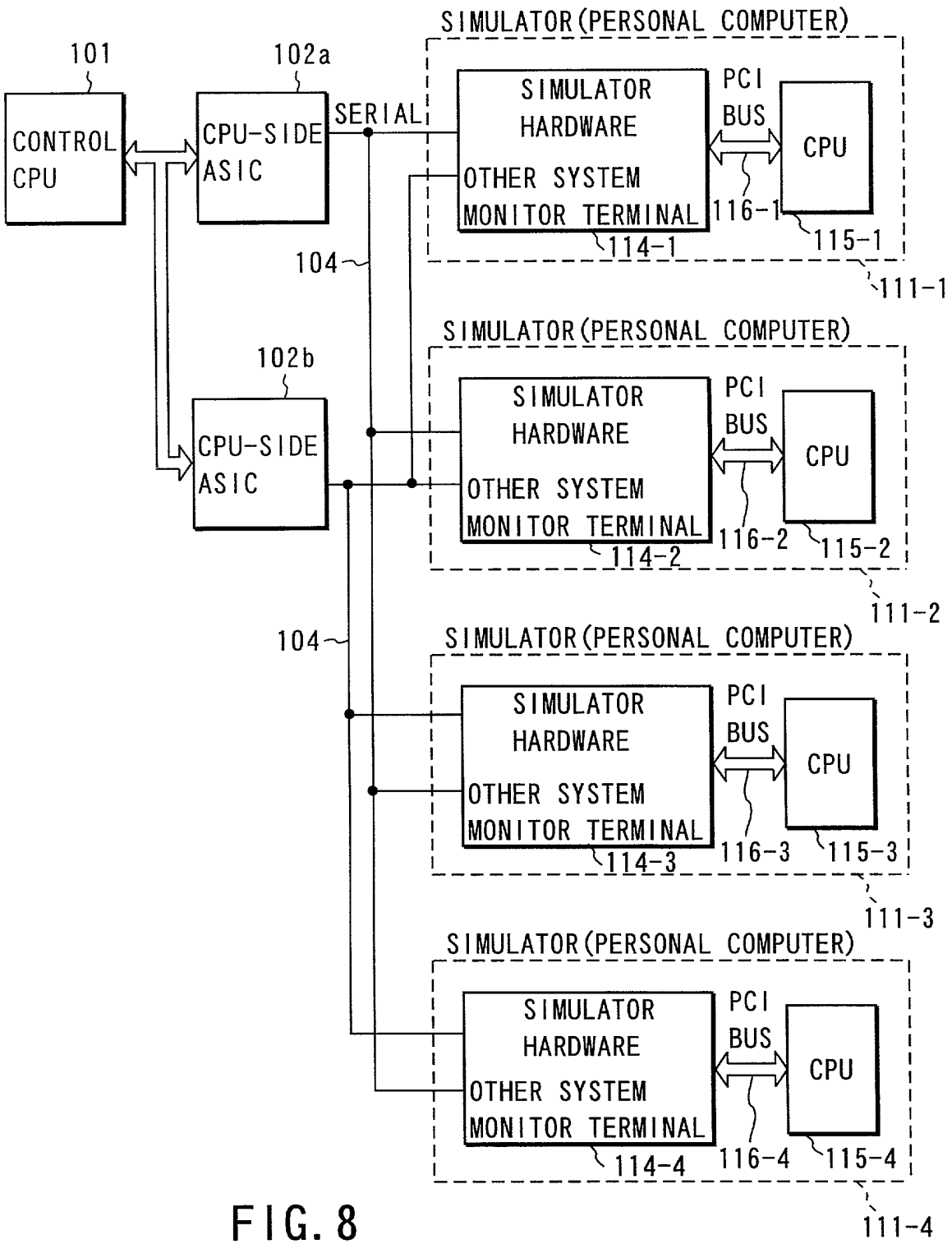
SIMULATOR(PERSONAL COMPUTER)
101
102a
CONTROL CPU
CPU-SIDE ASIC
SERIAL
SIMULATOR HARDWARE
PCI BUS
CPU
OTHER SYSTEM MONITOR TERMINAL
116-1
115-1
114-1
104
111-1
SIMULATOR(PERSONAL COMPUTER)
102b
CPU-SIDE ASIC
SIMULATOR HARDWARE
PCI BUS
CPU
OTHER SYSTEM MONITOR TERMINAL
116-2
115-2
114-2
111-2
104
SIMULATOR(PERSONAL COMPUTER)
SIMULATOR HARDWARE
PCI BUS
CPU
OTHER SYSTEM MONITOR TERMINAL
116-3
115-3
114-3
111-3
SIMULATOR(PERSONAL COMPUTER)
SIMULATOR HARDWARE
PCI BUS
CPU
OTHER SYSTEM MONITOR TERMINAL
116-4
115-4
114-4
111-4

FIG. 8

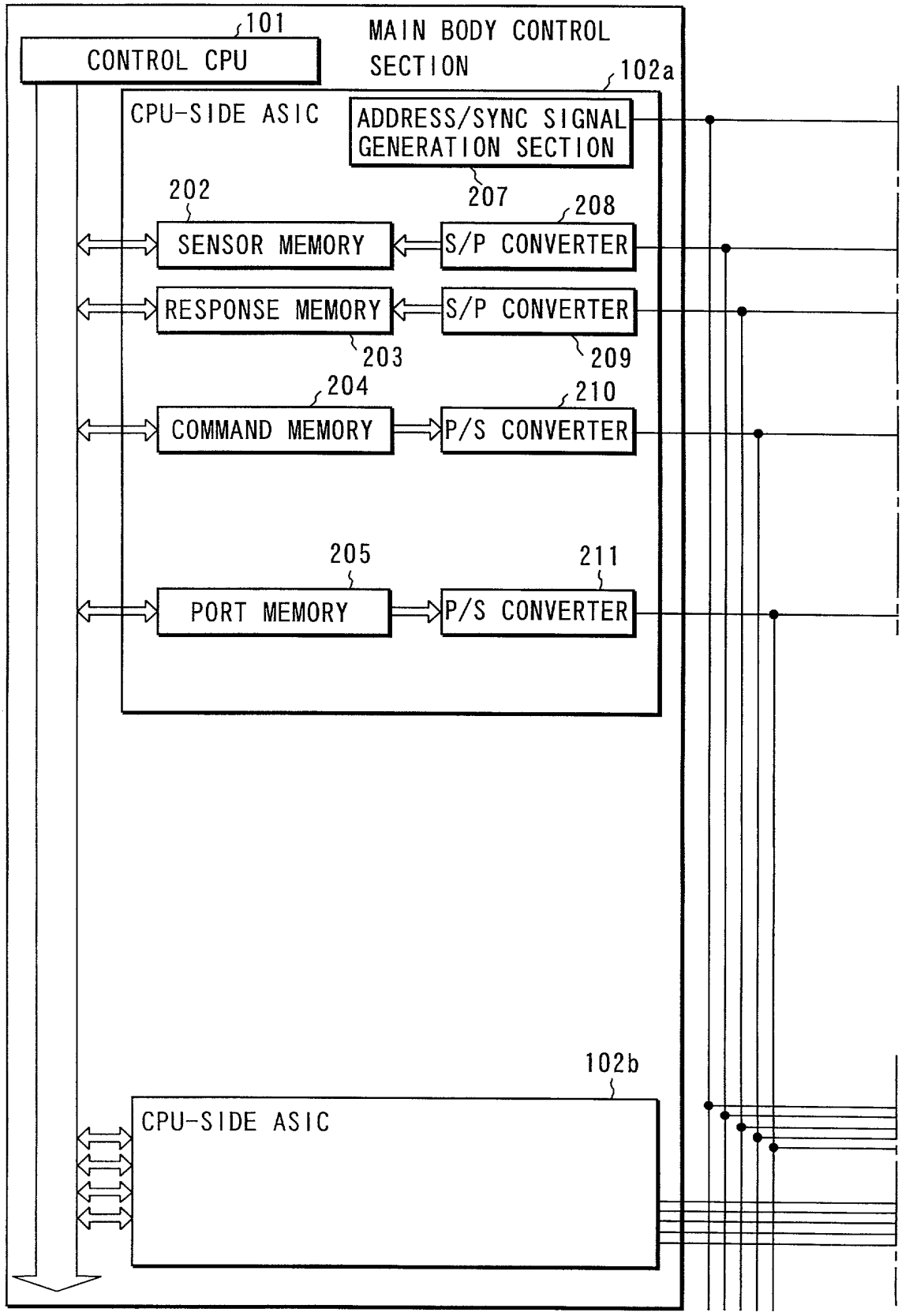
101
CONTROL CPU
MAIN BODY CONTROL SECTION
102a
CPU-SIDE ASIC
ADDRESS/SYNC SIGNAL GENERATION SECTION
207
202
208
SENSOR MEMORY
S/P CONVERTER
RESPONSE MEMORY
S/P CONVERTER
203
209
204
210
COMMAND MEMORY
P/S CONVERTER
205
211
PORT MEMORY
P/S CONVERTER
102b
CPU-SIDE ASIC

FIG. 9A

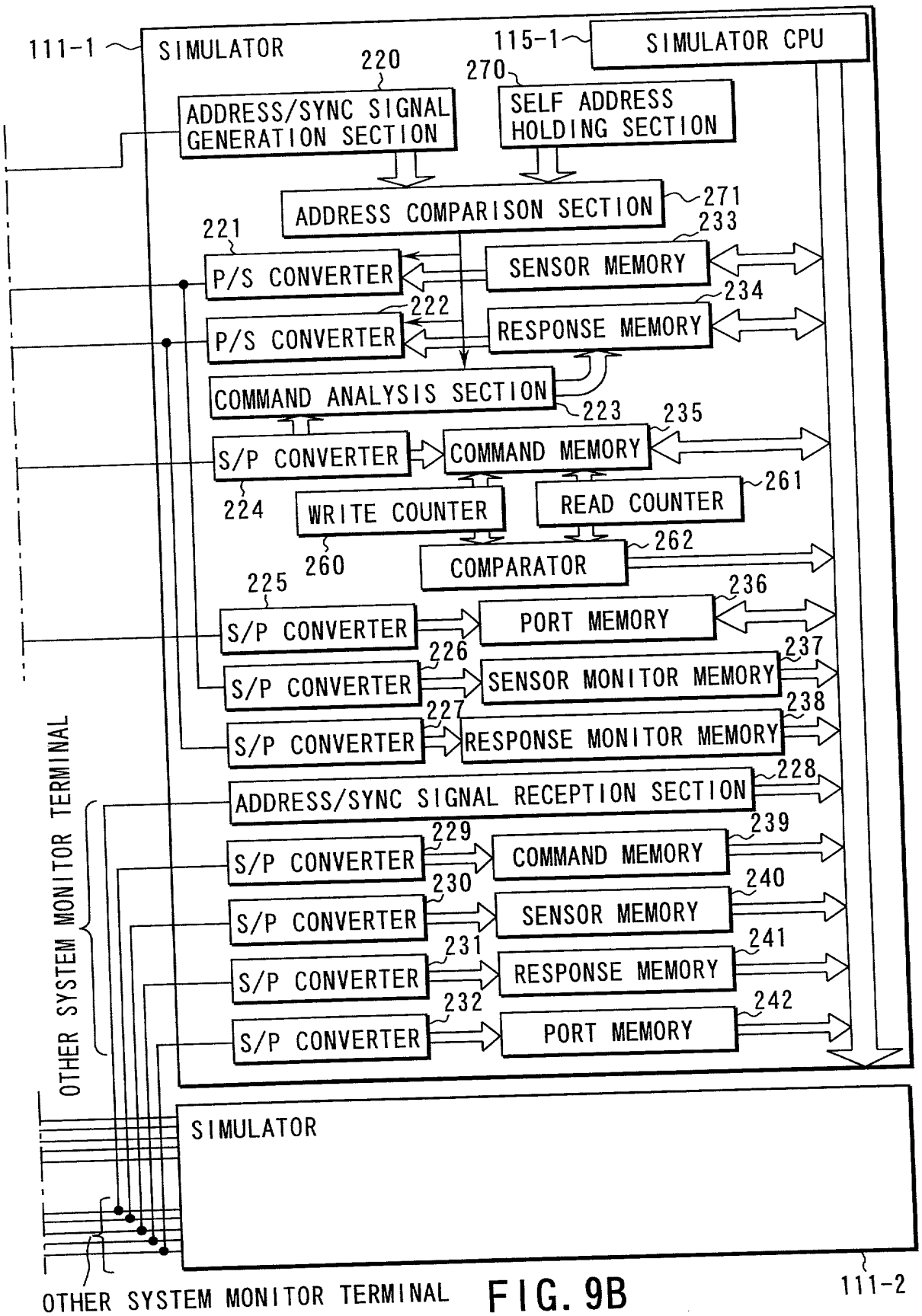
111-1
SIMULATOR
115-1
SIMULATOR CPU
220
ADDRESS/SYNC SIGNAL GENERATION SECTION
270
SELF ADDRESS HOLDING SECTION
ADDRESS COMPARISON SECTION
271
221
P/S CONVERTER
233
SENSOR MEMORY
222
P/S CONVERTER
234
RESPONSE MEMORY
COMMAND ANALYSIS SECTION
223
235
S/P CONVERTER
COMMAND MEMORY
224
WRITE COUNTER
READ COUNTER
261
260
COMPARATOR
262
225
S/P CONVERTER
PORT MEMORY
236
226
S/P CONVERTER
SENSOR MONITOR MEMORY
237
227
S/P CONVERTER
RESPONSE MONITOR MEMORY
238
ADDRESS/SYNC SIGNAL RECEPTION SECTION
228
229
S/P CONVERTER
COMMAND MEMORY
239
230
S/P CONVERTER
SENSOR MEMORY
240
231
S/P CONVERTER
RESPONSE MEMORY
241
232
S/P CONVERTER
PORT MEMORY
242
OTHER SYSTEM MONITOR TERMINAL
SIMULATOR
OTHER SYSTEM MONITOR TERMINAL
111-2

FIG. 9B

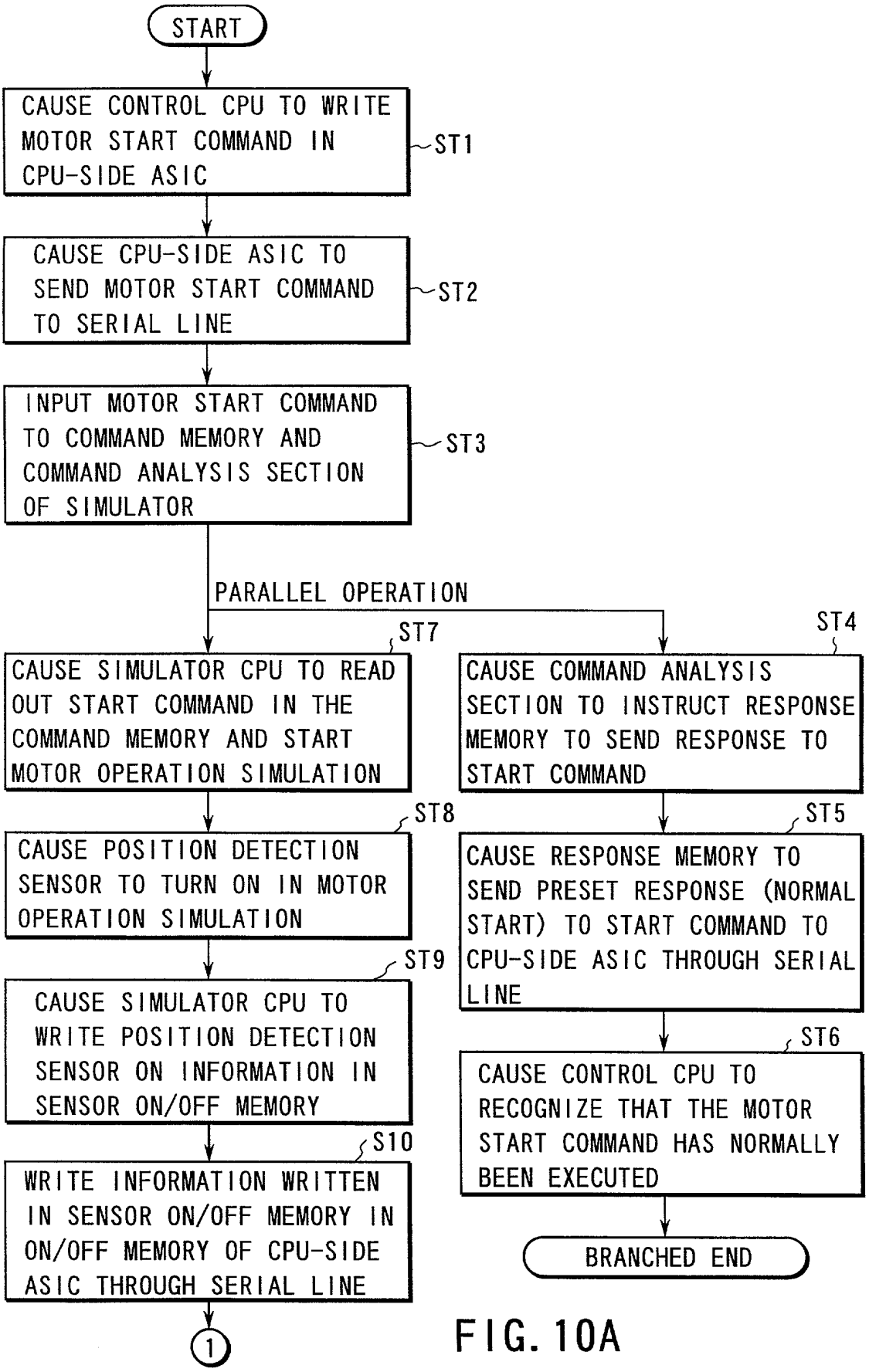
START
CAUSE CONTROL CPU TO WRITE MOTOR START COMMAND IN CPU-SIDE ASIC
ST1
CAUSE CPU-SIDE ASIC TO SEND MOTOR START COMMAND TO SERIAL LINE
ST2
INPUT MOTOR START COMMAND TO COMMAND MEMORY AND COMMAND ANALYSIS SECTION OF SIMULATOR
ST3
PARALLEL OPERATION
ST7
CAUSE SIMULATOR CPU TO READ OUT START COMMAND IN THE COMMAND MEMORY AND START MOTOR OPERATION SIMULATION
ST4
CAUSE COMMAND ANALYSIS SECTION TO INSTRUCT RESPONSE MEMORY TO SEND RESPONSE TO START COMMAND
ST8
CAUSE POSITION DETECTION SENSOR TO TURN ON IN MOTOR OPERATION SIMULATION
ST5
CAUSE RESPONSE MEMORY TO SEND PRESET RESPONSE (NORMAL START) TO START COMMAND TO CPU-SIDE ASIC THROUGH SERIAL LINE
ST9
CAUSE SIMULATOR CPU TO WRITE POSITION DETECTION SENSOR ON INFORMATION IN SENSOR ON/OFF MEMORY
ST6
CAUSE CONTROL CPU TO RECOGNIZE THAT THE MOTOR START COMMAND HAS NORMALLY BEEN EXECUTED
S10
WRITE INFORMATION WRITTEN IN SENSOR ON/OFF MEMORY IN ON/OFF MEMORY OF CPU-SIDE ASIC THROUGH SERIAL LINE
BRANCHED END
1

FIG. 10A

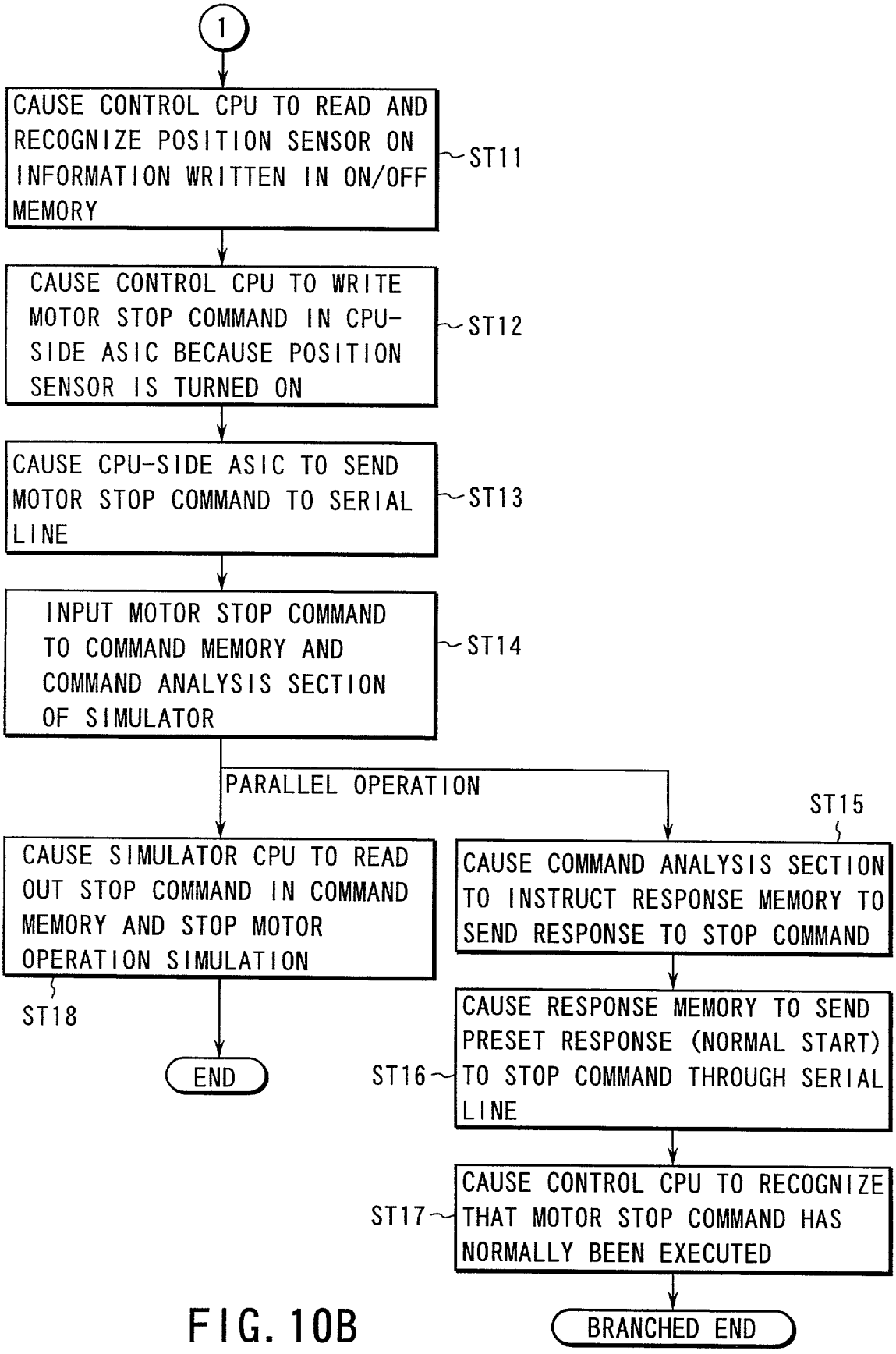
1
CAUSE CONTROL CPU TO READ AND RECOGNIZE POSITION SENSOR ON INFORMATION WRITTEN IN ON/OFF MEMORY
ST11
CAUSE CONTROL CPU TO WRITE MOTOR STOP COMMAND IN CPU-SIDE ASIC BECAUSE POSITION SENSOR IS TURNED ON
ST12
CAUSE CPU-SIDE ASIC TO SEND MOTOR STOP COMMAND TO SERIAL LINE
ST13
INPUT MOTOR STOP COMMAND TO COMMAND MEMORY AND COMMAND ANALYSIS SECTION OF SIMULATOR
ST14
PARALLEL OPERATION
CAUSE SIMULATOR CPU TO READ OUT STOP COMMAND IN COMMAND MEMORY AND STOP MOTOR OPERATION SIMULATION
ST18
END
ST15
CAUSE COMMAND ANALYSIS SECTION TO INSTRUCT RESPONSE MEMORY TO SEND RESPONSE TO STOP COMMAND
CAUSE RESPONSE MEMORY TO SEND PRESET RESPONSE (NORMAL START) TO STOP COMMAND THROUGH SERIAL LINE
ST16
CAUSE CONTROL CPU TO RECOGNIZE THAT MOTOR STOP COMMAND HAS NORMALLY BEEN EXECUTED
ST17
BRANCHED END

FIG. 10B

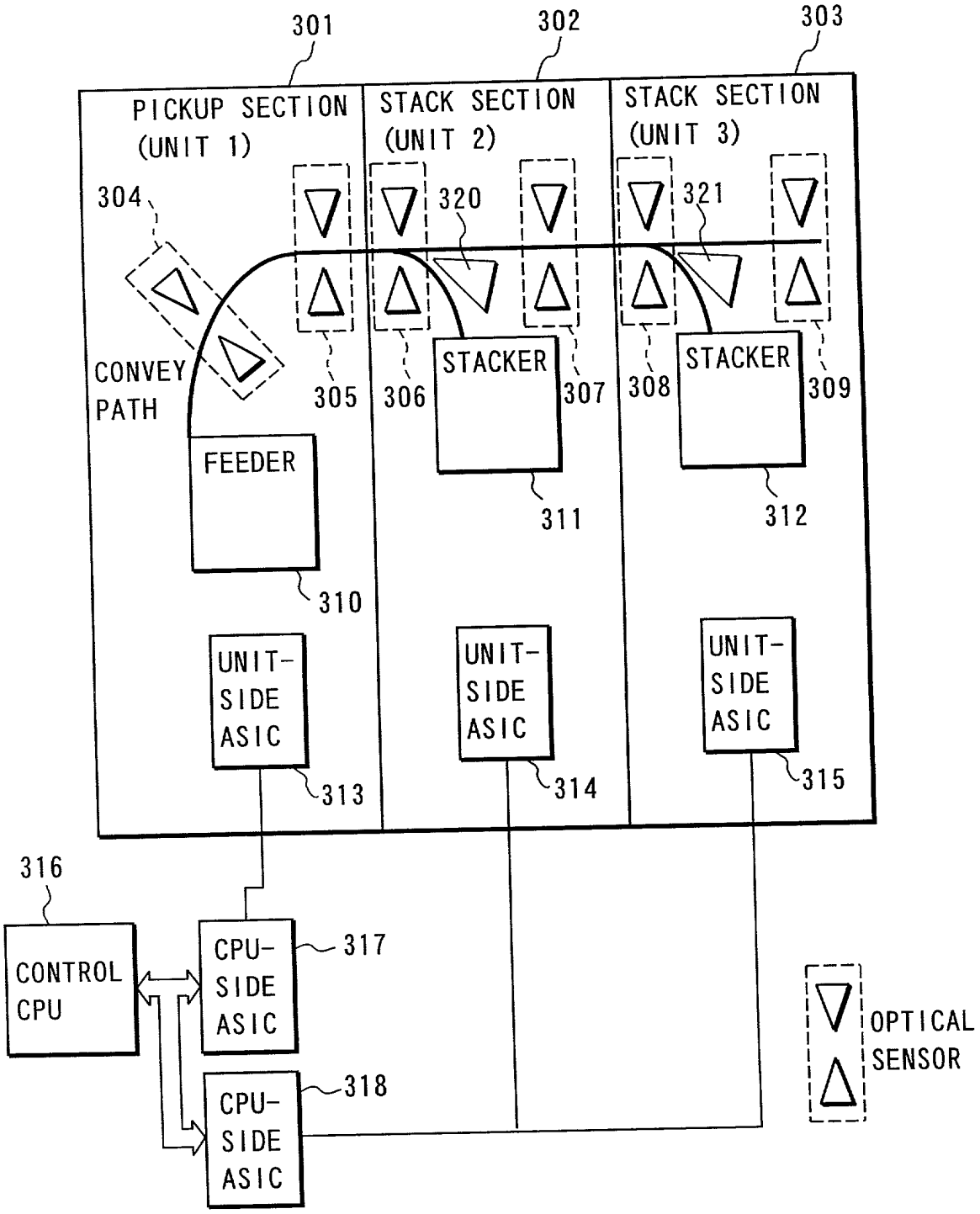
301
302
303
PICKUP SECTION
(UNIT 1)
STACK SECTION
(UNIT 2)
STACK SECTION
(UNIT 3)
304
320
321
CONVEY
PATH
305
306
STACKER
307
308
STACKER
309
FEEDER
310
311
312
UNIT-
SIDE
ASIC
313
UNIT-
SIDE
ASIC
314
UNIT-
SIDE
ASIC
315
316
CONTROL
CPU
CPU-
SIDE
ASIC
317
CPU-
SIDE
ASIC
318
OPTICAL
SENSOR

FIG. 11

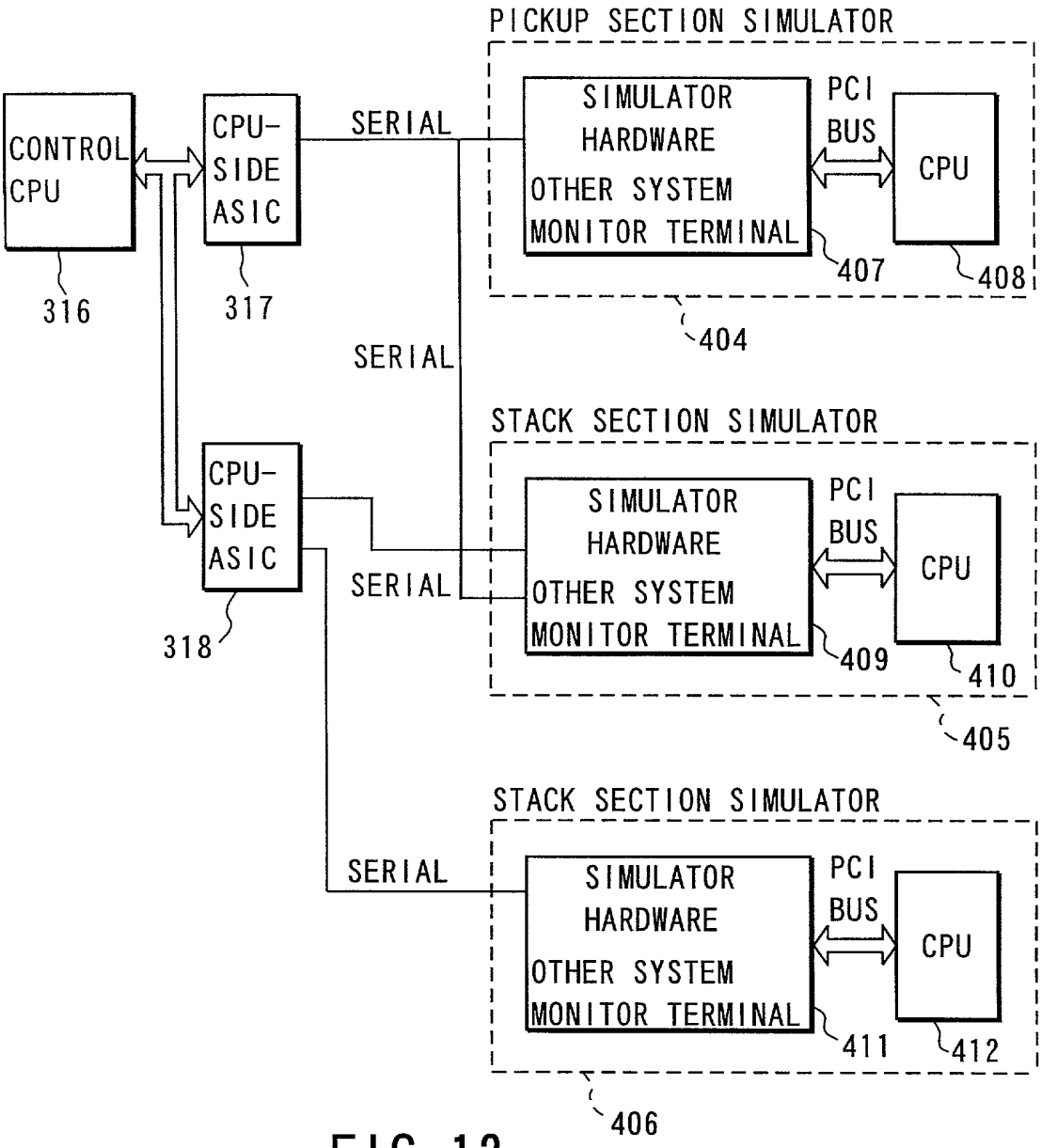
PICKUP SECTION SIMULATOR
CONTROL CPU
CPU-SIDE ASIC
SERIAL
SIMULATOR HARDWARE
OTHER SYSTEM MONITOR TERMINAL
PCI BUS
CPU
316
317
407
408
404
SERIAL
STACK SECTION SIMULATOR
CPU-SIDE ASIC
SERIAL
SIMULATOR HARDWARE
OTHER SYSTEM MONITOR TERMINAL
PCI BUS
CPU
318
409
410
405
STACK SECTION SIMULATOR
SERIAL
SIMULATOR HARDWARE
OTHER SYSTEM MONITOR TERMINAL
PCI BUS
CPU
411
412
406

FIG. 12

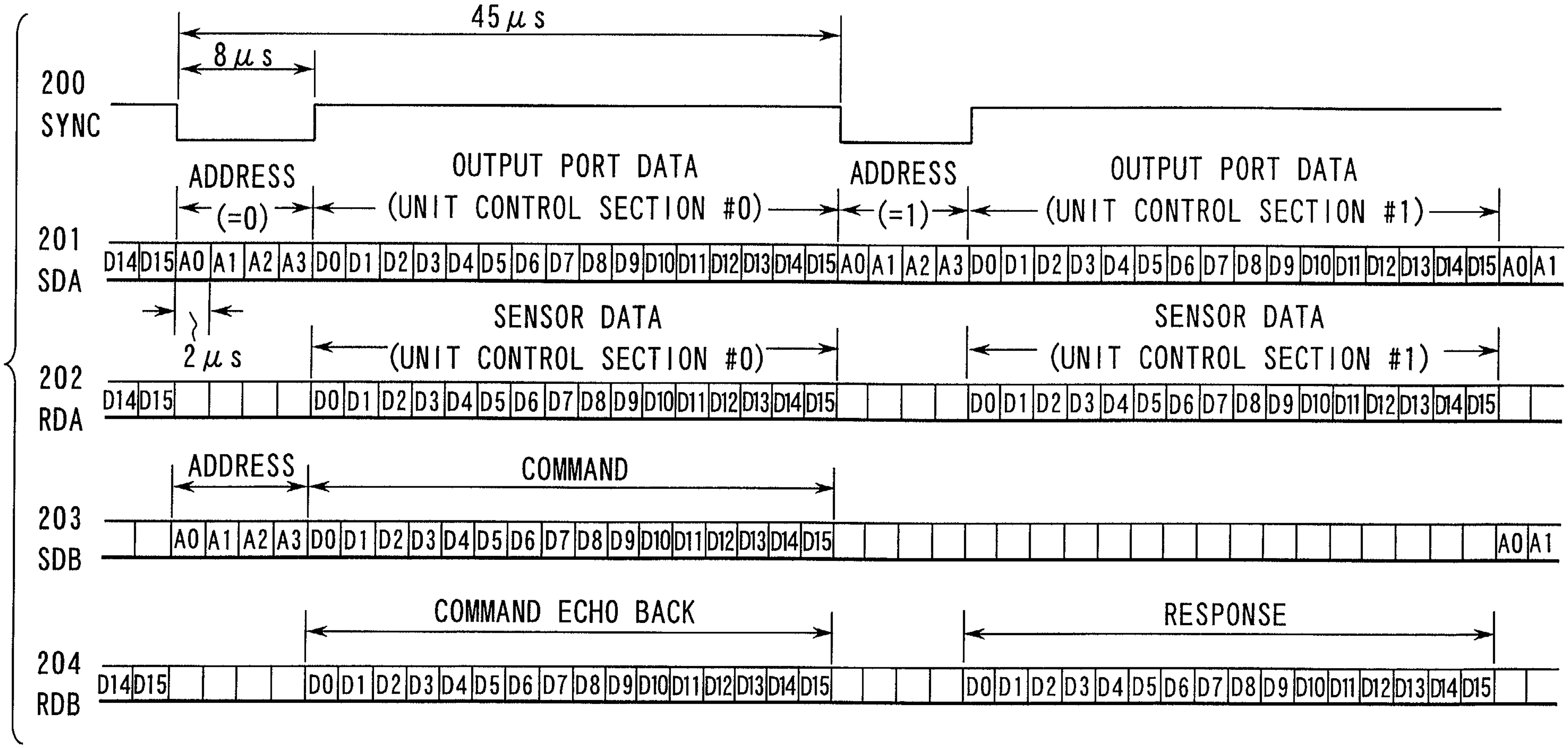
200
SYNC
201
SDA
202
RDA
203
SDB
204
RDB
45 μs
8 μs
2 μs
ADDRESS (=0)
OUTPUT PORT DATA (UNIT CONTROL SECTION #0)
ADDRESS (=1)
OUTPUT PORT DATA (UNIT CONTROL SECTION #1)
SENSOR DATA (UNIT CONTROL SECTION #0)
SENSOR DATA (UNIT CONTROL SECTION #1)
ADDRESS
COMMAND
COMMAND ECHO BACK
RESPONSE
D14 D15 A0 A1 A2 A3 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 A0 A1 A2 A3 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 A0 A1

FIG. 13

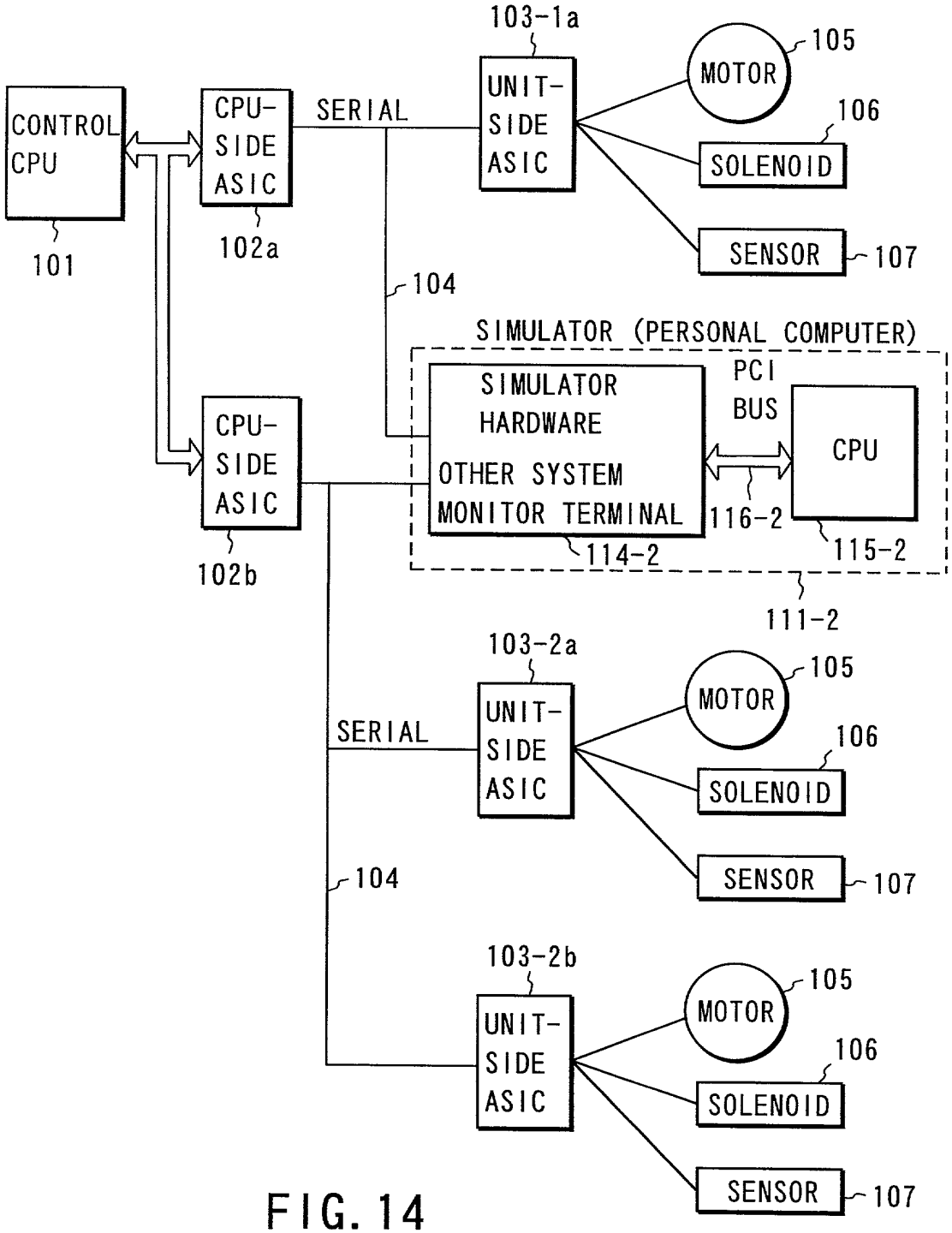
CONTROL CPU
101
CPU-SIDE ASIC
102a
SERIAL
103-1a
UNIT-SIDE ASIC
MOTOR
105
106
SOLENOID
SENSOR
107
104
SIMULATOR (PERSONAL COMPUTER)
SIMULATOR HARDWARE
OTHER SYSTEM MONITOR TERMINAL
114-2
PCI BUS
CPU
116-2
115-2
111-2
CPU-SIDE ASIC
102b
SERIAL
103-2a
UNIT-SIDE ASIC
MOTOR
105
106
SOLENOID
SENSOR
107
104
103-2b
UNIT-SIDE ASIC
MOTOR
105
106
SOLENOID
SENSOR
107

FIG. 14